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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/770,919	02/03/2004	Chad A. Cobbley	MICS:0078-5	1688
52142 7590 01/23/2008 FLETCHER YODER (MICRON TECHNOLOGY, INC.) P.O. BOX 692289 HOUSTON, TX 77269-2289			EXAMINER MITCHELL, JAMES M	
			ART UNIT 2813	PAPER NUMBER
			MAIL DATE 01/23/2008	DELIVERY MODE PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/770,919	<b>Applicant(s)</b> COBBLEY ET AL.	
	<b>Examiner</b> James M. Mitchell	<b>Art Unit</b> 2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 23 March 2007.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) 3,4 and 16-21 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,2 and 5-15 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### DETAILED ACTION

1. This office action is response to applicant's appeal brief filed March 23, 2007.

#### ***Claim Rejections - 35 USC § 112***

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1, 2 and 5-15 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The definition of a substrate is a supporting material on or **in which** the components of an integrated circuit are **fabricated or attached**, or an insulating layer that components are formed on; therefore, since the dies contain circuits formed in semiconductor substrates the stack includes a substrate. Alternatively, the die stacks are formed on/ attached to a holder albeit temporarily and therefore the holder is still within the definition of a substrate. As such, the claim is not enabled, since one skilled in the art to which it pertains, or with which it is most nearly connected, cannot make a stack formed on *what it excludes*<sup>1</sup>.

4. Claims 1, 2 and 5-15 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to

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<sup>1</sup> For examination, no substrate is interpreted to mean a die stack without a permanent substrate.

one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. There is no support in the specification for the negative limitation that the die stacks do not include a lead frame.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 1, 2 and 5-15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. The term "configured," while applicant's specification makes mention of the configuration of chips (e.g. different sizes etc.) it is completely silent as to how the "holder is **configured**..." except to say, "[t]he holding surface is considered temporary in that the wafer itself may be used to temporarily hold, transfer, test or store one or more die stacks **for example**." There is nothing in the specification that would apprise one of the metes and bounds of how the substrate was configured<sup>2</sup> or the structural limitations imparted.

***Claim Rejections - 35 USC § 102***

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1 and 5 are rejected under 35 U.S.C. 102(b) as being anticipated by Fujimoto (JP 6,255,726).

10. Fujimoto discloses:

(cl. 1) a plurality of semiconductor die stacks thereon (4; Fig. 1a), wherein each of the plurality of semiconductor die stacks include at least two semiconductor die (4) coupled together by an adhesive (2) and wherein the plurality of semiconductor die stacks do not include a lead frame (e.g. none shown) or a substrate (e.g. tape is temporary);

(cl. 5) at least three dies connected by adhesives (2; Fig. 1)

***Claim Rejections - 35 USC § 103***

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

12. Claims 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujimoto (JP 6,255,726).

13. Fujimoto discloses the claimed elements in paragraph 10 of this office action, but does not appear to show a shingle stack, that the one die is thicker than another die of a second stack or that one topside surface of one chip is less than the topside surface of another chip.

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<sup>2</sup> Note, a substrate/PCB that a chip is soldered may be considered temporary in that the chip may be

14. With respect to the shingle stack (understood to mean offset) of claim 8, applicant has not disclosed that the offset of dies modifies the operation. As such, the rearrangement would have been obvious to one of ordinary skill in the art, since it has been held that the shifting of positions of parts is unpatentable where the operation is not modified. In re Japikse, 181 F.2d 1019, 86 USPQ 70 (CCPA 1950) (Claims to a hydraulic power press which read on the prior art except with regard to the position of the starting switch were held unpatentable because shifting the position of the starting switch would not have modified the operation of the device.); In re Kuhle, 526 F.2d 553, 188 USPQ 7 (CCPA 1975) (the particular placement of a contact in a conductivity measuring device was held to be an obvious matter of design choice).

15. With respect the claimed dimensions, applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. As such, it would have been obvious to one of ordinary skill in the art to form the chips with the claimed sizes, since it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

16. Claims 2, 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujimoto (JP 6,255,726) in combination with Yajima (J.P. 362048037).

17. Fujimoto discloses the elements stated in paragraph 10 of this office action, but does not explicitly disclose the die stacks on a tape reel.

18. However Yajima utilizes a tape reel (21).

19. It would have been obvious to one of ordinary skill in the art to form the dies of Fujimoto on a tape reel (e.g. wound in a roller) in order to convey the semiconductor material as taught by Yajima (Eng. Abstract).

20. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fujimoto (JP 6,255,726) in combination with Ang (U.S. 6,599,764).

21. Fujimoto discloses the elements stated in paragraph 10 of this office action, but fails to explicitly disclose its die/chips as memory.

22. However, Ang (e.g. Col. 4, Line 10) utilizes a memory chips.

23. It would have been obvious to one of ordinary skill in the art to form the chips of Fujimoto with memory in order to provide logic components and type of chip as taught by Ang (Col. 4, line 10).

24. Claims 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujimoto (JP 6,255,726) in combination with Yajima (J.P. 362048037).

25. Fujimoto and Yajima discloses the claimed elements in paragraphs 17-19 of this office action, but does not appear to show a shingle stack, that the one die is thicker

than another die of a second stack or that one topside surface of one chip is less than the topside surface of another chip.

26. With respect to the shingle stack (understood to mean offset) of claim 14, applicant has not disclosed that the offset of dies modifies the operation. As such, the rearrangement would have been obvious to one of ordinary skill in the art, since it has been held that the shifting of positions of parts is unpatentable where the operation is not modified. In re Japikse, 181 F.2d 1019, 86 USPQ 70 (CCPA 1950) (Claims to a hydraulic power press which read on the prior art except with regard to the position of the starting switch were held unpatentable because shifting the position of the starting switch would not have modified the operation of the device.); In re Kuhle, 526 F.2d 553, 188 USPQ 7 (CCPA 1975) (the particular placement of a contact in a conductivity measuring device was held to be an obvious matter of design choice).

27. With respect the claimed dimensions, applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. As such, it would have been obvious to one of ordinary skill in the art to form the chips with the claimed sizes, since it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).



28. Claims 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fujimoto (JP 6,255,726) and Yajima (J.P. 362048037) as applied to claim 10 and further in combination with Ang (U.S. 6,599,764).

29. Neither Fujimoto nor Yajima explicitly discloses its die/chips as memory.

30. However, Ang (e.g. Col. 4, Line 10) discloses memory chips.

31. It would have been obvious to one of ordinary skill in the art to form the chips of Fujimoto with memory in order to provide logic components and a type of chip as taught by Ang (Col. 4, line 10).

#### ***Response to Arguments***

32. Upon further examination of the prior art, examiner concurs with applicant's assertion that Bjork has a substrate precluding it from reading on a claim requiring no substrate. Similarly examiner finds that Ang does not disclose or make obvious an adhesive between two chips, since Ang discloses that only one chip is attached to the protective layer. However, applicant's remarks are moot in view of the new ground(s) of rejection. Based on the indicated differences, the finality of the last office action is withdrawn.

#### ***Conclusion***

33. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The prior art discloses a die stack on a temporary holder/substrate, and the use of a dicing tape on a reel.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to James M. Mitchell whose telephone number is (571) 272-1931. The examiner can normally be reached on M-F 8:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Ex. Mitchell  
January 21, 2008



Carl Whitehead Jr.  
EBC Art 2813